Electronic Version
Stylesheet Version v1.1.1

Description

[ELECTROSTATIC DISCHARGE PROTECTION DEVICE]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention is related to an electrostatic discharge (ESD) protection device. More particularly, the present invention relates to an ESD protection device for bypassing an ESD current with low-capacitance and low substrate noise.

[0003] Description of Related Art

[0004] As the semiconductor technology advances, the integration of the semiconductor devices are enhanced by, for example, reducing the line width and increasing the stacked layers of the semiconductor device. However, as the area and the tolerance of the integrated circuits (IC) reduce, the damage caused by the electrostatic discharge (ESD) could become a serious problem. Conventionally,

the waveform of the electrostatic discharge (ESD) has the properties of short rise time (e.g., generally between 5ns to 15ns) and high pulse power (e.g., generally between 1000V to 3000V). Therefore, when the integrated circuit (IC) is damaged by the ESD, the IC might get punched through or burned out suddenly.

[0005] Therefore, in order to resolve the problems described above, an ESD protection circuit is generally disposed between the input and output pads of the IC to protect the IC from the ESD damage by shunting the electrostatic charges of the ESD source from the IC. Specially, the ESD protection circuit impacts the performance of the radio frequency (RF) IC (e.g., the signal integrity, input/output (I/O) impedance matching, power efficiency and bandwidth etc.) due to the sizeable ESD induced parasitics such as the parasitic resistance and capacitance associated with the ESD protection circuit. In addition, the ESD protection circuit also introduce noise coupling due to parasitic capacitance and will generate extra noises that will affect total IC noise figures.

[0006] FIG. 1A is a schematic circuit diagram of a conventional radio frequency (RF) ESD protection circuit. Referring to FIG. 1A, an ESD protection circuit 100 including a PMOS

transistor 104, an NMOS transistor 106 and a diode string 110 is connected to an input/output (I/O) pad 108 and is connected between voltages V_{DD} and V_{SS} of RF IC 102. The gate of the PMOS transistor 104 and the NMOS transistor 106 are connected to the pad 108, the source of the PMOS transistor 104 is connected to the drain of the NMOS transistor 106, the drain of the PMOS transistor 104 is connected to the voltage V_{DD}, and the source of the NMOS transistor 106 is connected to the voltage V_{SS}. The diode string 110 includes m diodes (i.e., diodes 112a to 112m) connected between the voltage V_{DD} and the pad 108 and n diodes (i.e., diodes 114a to 114n) connected between the voltage V_{SS} and the pad 108. The PMOS transistor 104 and the NMOS transistor 106 are provided for bypassing the ESD current. In addition, a portion of the ESD current may also be shunted from the diodes 112a to 112m or the diodes 114a to 114n of the diode string 110.

[0007] FIG. 1B is a schematic cross-sectional view illustrating the diode string of the RF ESD protection circuit shown in FIG. 1A. Referring to FIG. 1B, each of the diodes 112a to 112m and 114a to 114n may be constructed by a N-well region formed in a P-type substrate 101, and a highly doped N-type region (N+ region) and highly doped P-type region

(P+ region) formed in the N-well. It is noted that, although the diodes 112a to 112m or the diodes 114a to 114n of the diode string 110 may be used to bypass a portion of the ESD current, however, the parasitic capacitance of each diode in the diode string 110 is large. In general, the parasitic capacitance of each diode in the diode string 110 is associated with the parallel connection of the parasitic capacitance C1 between the P+ region and the N-well region and the parasitic capacitance C2 between the N-well region and the P-type substrate 101. It is noted that the parasitic capacitance C1 is much larger than the parasitic capacitance C2 since the area of the junction between the N-well region and the P-type substrate 101 is much larger than the area between the P+ region and the N-well region. Therefore, the parasitic capacitance of the series connection of diodes 112a to 112m is about (C1+C2)/m (m is the number of the diodes 112a to 112m). Similarly, the parasitic capacitance of the series connection of diodes 114a to 114n is about (C1+C2)/m (wherein m is the number of the diodes 114a to 114n). Thus, the parasitic capacitance of the diode string 110 is about (C1+C2)/(n+m). It is noted that, since the parasitic capacitance C1 is much larger than the para-

sitic capacitance C2, the parasitic capacitance of the diode string 110 is still large.

[0008] Therefore, the conventional RF ESD protection circuit 100 shown in FIG. 1A and FIG. 1B has the disadvantages that the parasitic capacitance of the diode string 110 is large. It is noted that, the transmission of the RF signal may be delayed due to the large parasitic capacitance of the diode string 110. Thus, the performance of the RF IC 102 is degraded or even failed.

[0009] In order to solve the problem described above, another conventional RF ESD protection circuit is developed. FIG. 2A is a schematic circuit diagram of another conventional RF ESD protection circuit. Referring to FIG. 2A, an ESD protection circuit 200 including a PMOS transistor 204, an NMOS transistor 206 and a diode string 210 is connected to an I/O pad 208 and is connected between voltages V_{DD} and V_{SS} of RF IC 202. The gate of the PMOS transistor 204 and the NMOS transistor 206 are connected to the pad 208, the source of the PMOS transistor 204 is connected to the drain of the NMOS transistor 206, the drain of the PMOS transistor 204 is connected to the voltage V_{DD}, and the source of the NMOS transistor 206 is connected to the voltage V_{SS}. The diode string 210 includes a plurality of

diodes 212a to 212m connected between the voltage V_{DD} and the pad 208 and a diode 214 connected between the voltage V_{SS} and the pad 208.

[0010] FIG. 2B is a schematic cross-sectional view illustrating the diode string of the RF ESD protection circuit shown in FIG. 2A. Referring to FIG. 2B, each of the diodes 212a to 212m may be constructed by a N-well region formed in a P-type substrate 201, and an N+ region and a P+ region formed in the N-well region. In addition, the diode 214 is constructed by an N+ region, a P+ region and the P-type substrate 201. It is noted that, when FIG. 1B and FIG. 2B are under similar process parameters and structure dimensions, the parasitic capacitance C3 of the diode 214 is close to the parasitic capacitance C1 since the area of the junction between the N+ region and the P-type substrate 201 in the diode 214 is close to the area of the junction between the P+ region and the N-well region in the diode 114a. Therefore, the parasitic capacitance C3 of the diode 214 shown in FIG. 1B is less than the parasitic capacitance (C1+C2)/m of the series connection of the diodes 114a to 114n. Therefore, the parasitic capacitance of the diode string 210 is less than that of the diode string 110.

[0011] It is noted that, in FIG. 2B, although the parasitic capaci-

tance of the diode string 210 is reduced, however, a substrate noise generated from other circuits in the same substrate 201 may be coupled into the RF input mode through the diode 214 constructed by the P-type substrate 201. Therefore, the performance of the RF IC 102 is seriously degraded by the substrate noise. Accordingly, an ESD protection circuit with low-capacitance and low substrate noise is quite desirable.

SUMMARY OF INVENTION

[0012] Accordingly, the present invention is directed to electrostatic discharge (ESD) protection device with low-capacitance and low substrate noise capable of bypassing an ESD current.

[0013] In addition, the present invention is also directed to electrostatic discharge (ESD) protection circuit low-capacitance and low substrate noise capable of bypassing an ESD current.

[0014] According to one embodiment of the present invention, an electrostatic discharge (ESD) protection device comprising an ESD clamp circuit is provided. The ESD clamp circuit comprises, for example but not limited to, at least a diode connected in series between a first voltage and a pad, and at least an ESD component connected in series between a

second voltage and a pad. Each of the at least an ESD component comprises a deep N-well region formed in a P-type substrate, a triple P-well formed in the deep N-well region, and a highly doped N-type (N+) region and a highly doped P-type (P+) region formed in the triple P-well region.

[0015] In one embodiment of the present invention, when a number of the ESD component is one, the N+ region of the ESD component is connected to the pad, and the P+ region of the ESD component is connected to the second voltage.

[0016] In one embodiment of the present invention, when a number of the ESD component is two including a 1^{st} ESD component and a 2^{nd} ESD component, the N+ region of a 1^{st} ESD component is connected to the pad, the P+ region of the 2^{nd} ESD component is connected to the second voltage, and the P+ region of the 1^{st} ESD component is connected to the N+ region of the 2^{nd} ESD component.

[0017] In one embodiment of the present invention, when a number of the ESD component is S including a 1^{st} ESD component to a S^{th} ESD component, the N+ region of the 1^{st} ESD component is connected to the pad, the P+ region of the S^{th} ESD component is connected to the second volt-

age, and the P+ region of the T^{th} ESD component is connected to the N+ region of the $(T+1)^{th}$ ESD component, wherein S is a positive integer and T is a positive integer from 1 to S-1.

[0018] In one embodiment of the present invention, each of the at least a diode comprises a N-well region formed in a P-type substrate, and a N+ region and a P+ region formed in the N-well region.

[0019] In one embodiment of the present invention, when a number of the diode is one, the N+ region of the diode is connected to the first voltage, and the P+ region of the diode is connected to the pad.

[0020] In one embodiment of the present invention, when a number of the diode is two including a first diode and a second diode, the N+ region of a first diode is connected to the first voltage, the P+ region of the second diode is connected to the pad, and the P+ region of the first diode is connected to the N+ region of the second diode.

[0021] In one embodiment of the present invention, when a number of the diode is S including a 1^{st} diode to a S^{th} diode, the N+ region of the 1^{st} diode is connected to the first voltage, the P+ region of the S^{th} diode is connected to the pad, and the P+ region of the T^{th} diode is con-

nected to the N+ region of the $(T+1)^{th}$ diode, wherein S is a positive integer and T is a positive integer from 1 to S-1.

[0022] In one embodiment of the present invention, the ESD protection circuit further comprises another ESD clamp circuit comprising a PMOS transistor and an NMOS transistor. A gate of the PMOS transistor and a gate of the NMOS transistor are connected to the pad, a source of the PMOS transistor is connected to a drain of the NMOS transistor, a drain of the PMOS transistor is connected to the first voltage, and a source of the NMOS transistor is connected to the second voltage.

[0023] In one embodiment of the present invention, the ESD protection device is a radio frequency (RF) ESD protection device.

[0024] According to another embodiment of the present invention, an electrostatic discharge (ESD) protection device comprising an ESD clamp circuit is provided. The ESD clamp circuit comprises, for example but not limited to, at least a first ESD component connected in series between a first voltage and a pad, and at least a second ESD component connected in series between a second voltage and a pad. Each of the at least a first ESD component or the at

least a first ESD component comprises a deep N-well region formed in a P-type substrate, a triple P-well formed in the deep N-well region, and a highly doped N-type (N+) region and a highly doped P-type (P+) region formed in the triple P-well region.

[0025] In one embodiment of the present invention, when a number of the first ESD component is one, the N+ region of the first ESD component is connected to the pad, and the P+ region of the first ESD component is connected to the second voltage.

[0026] In one embodiment of the present invention, when a number of the first ESD component is two including a 1^{st} first ESD component and a 2^{nd} first ESD component, the N+ region of a 1^{st} first ESD component is connected to the pad, the P+ region of the 2^{nd} first ESD component is connected to the second voltage, and the P+ region of the 1^{st} first ESD component is connected to the N+ region of the 2^{nd} first ESD component.

[0027] In one embodiment of the present invention, when a number of the first ESD component is S including a 1^{st} first ESD component to a S^{th} first ESD component, the N+ region of the 1^{st} first ESD component is connected to the pad, the P+ region of the S^{th} first ESD component is con-

nected to the second voltage, and the P+ region of the T^{th} first ESD component is connected to the N+ region of the $(T+1)^{th}$ first ESD component, wherein S is a positive integer and T is a positive integer from 1 to S-1.

[0028] In one embodiment of the present invention, when a number of the second ESD component is one, the N+ region of the second ESD component is connected to the first voltage, and the P+ region of the second ESD component is connected to the pad.

[0029] In one embodiment of the present invention, when a number of the second ESD component is two including a 1^{st} second ESD component and a 2^{nd} second ESD component, the N+ region of a 1^{st} second ESD component is connected to the first voltage, the P+ region of the 2^{nd} second ESD component is connected to the pad, and the P+ region of the 1^{st} second ESD component is connected to the N+ region of the 2^{nd} second ESD component.

[0030] In one embodiment of the present invention, when a number of the second ESD component is S including a 1^{st} second ESD component to a S^{th} second ESD component, the N+ region of the 1^{st} second ESD component is connected to the first voltage, the P+ region of the S^{th} second ESD component is connected to the pad, and the P+ re-

gion of the T^{th} second ESD component is connected to the N+ region of the $(T+1)^{th}$ second ESD component, wherein S is a positive integer and T is a positive integer from 1 to S-1.

[0031] In one embodiment of the present invention, the ESD protection circuit further comprises another ESD clamp circuit comprising a PMOS transistor and an NMOS transistor. A gate of the PMOS transistor and a gate of the NMOS transistor are connected to the pad, a source of the PMOS transistor is connected to a drain of the NMOS transistor, a drain of the PMOS transistor is connected to the first voltage, and a source of the NMOS transistor is connected to the second voltage.

[0032] In one embodiment of the present invention, the ESD protection device is a radio frequency (RF) ESD protection device.

[0033] Accordingly, since the ESD component is provided for the ESD clamp circuit of the ESD protection circuit of the present invention, the parasitic capacitance of the ESD clamp circuit is much less than that of the conventional diode string. In addition, since the ESD component dose not constructed by the substrate of the ESD clamp circuit of the ESD protection circuit, the problem of the substrate

noise may be reduced.

[0034] One or part or all of these and other features and advantages of the present invention will become readily apparent to those skilled in this art from the following description wherein there is shown and described a preferred embodiment of this invention, simply by way of illustration of one of the modes best suited to carry out the invention. As it will be realized, the invention is capable of different embodiments, and its several details are capable of modifications in various, obvious aspects all without departing from the invention. Accordingly, the drawings and descriptions will be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF DRAWINGS

[0035] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0036] FIG. 1A is a schematic circuit diagram of a conventional RF ESD protection circuit.

[0037] FIG. 1B is a schematic cross-sectional view illustrating the

diode string of the RF ESD protection circuit shown in FIG. 1A.

[0038] FIG. 2A is a schematic circuit diagram of another conventional RF ESD protection circuit.

[0039] FIG. 2B is a schematic cross-sectional view illustrating the diode string of the RF ESD protection circuit shown in FIG. 2A.

[0040] FIG. 3A is a schematic circuit diagram of a RF ESD protection circuit according to one embodiment of the present invention.

[0041] FIG. 3B is a schematic cross-sectional view illustrating the diode string of the RF ESD protection circuit according to one embodiment of the present invention.

[0042] FIG. 3C is a schematic circuit diagram of an ESD protection circuit according to one embodiment of the present invention.

[0043] FIG. 3D is a schematic cross-sectional view illustrating an ESD clamp circuit of an ESD protection circuit according to one embodiment of the present invention.

[0044] FIG. 4 is a diagram illustrating the parasitic capacitance of the ESD clamp circuit of the present invention and the conventional diode string versus the number of the ESD components or diodes thereof.

[0045] FIG. 5A is a schematic circuit diagram of a RF ESD protection circuit according to one embodiment of the present invention.

[0046] FIG. 5B is a schematic cross-sectional view illustrating the diode string of the RF ESD protection circuit according to one embodiment of the present invention.

[0047] FIG. 5C is a schematic circuit diagram of an ESD protection circuit according to one embodiment of the present invention.

[0048] FIG. 5D is a schematic cross-sectional view illustrating an ESD clamp circuit of an ESD protection circuit according to one embodiment of the present invention.

DETAILED DESCRIPTION

[0049] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

[0050] FIG. 3A is a schematic circuit diagram of an ESD protection circuit according to one embodiment of the present invention. Referring to FIG. 3A, an ESD protection circuit 300a comprises, for example but not limited to, an ESD clamp circuit 310a connected to an I/O pad 308 and connected between voltages V_{DD} and V_{SS} of IC 302. In one embodiment of the present invention, the voltages V_{DD} and V_{SS} represent a high voltage and a low voltage or vice versa. The ESD clamp circuit 310a comprises, for example but not limited to, at least a diode connected between voltage V_{DD} and the pad 308, and at least an ESD component connected between voltage V_{SS} and the pad 308.

[0051] FIG. 3B is a schematic cross-sectional view illustrating an ESD clamp circuit of an ESD protection circuit according to one embodiment of the present invention. Referring to FIG. 3A, at least two diodes 312a to 312m are connected in series between voltage V_{DD} and the pad 308, and at least two ESD components 314a to 314n are connected in series between voltage V_{SS} and the pad 308. Referring to FIG. 3B, each of the diodes 312a to 312m comprises, for example but not limited to, a N-well region formed in a P-type substrate 301, and a highly doped N-type region (N+ region) and a highly doped P-type region (P+ region)

formed in the N-well region. In one embodiment of the present invention, the ESD clamp circuit 310a may comprise only two diodes (e.g., diodes 312a and 312m). Thus, the P+ region of the diode 312a is connected to the pad 308, the N+ region of the diode 312m is connected to voltage V_{DD}, and the N+ region of the diode 312a is connected to the P+ region of the diode 312m. In one embodiment of the present invention, the ESD clamp circuit 310a may comprise more than two diodes (e.g., further comprises a diode 312b (not shown) connected between the N+ region of the diode 312a and the P+ region of the diode 312m). Thus, the P+ region of the diode 312b may be connected to the N+ region of the diode 312a, and the N+ region of the diode 312b may be connected to the P+ region of the diode 312m.

[0052] Referring to FIG. 3B, each of the ESD components 314a to 314n comprises, for example but not limited to, a deep N-well region formed in the P-type substrate 301, a triple P-well formed in the deep N-well region, and an N+ region and a P+ region formed in the triple P-well region. In one embodiment of the present invention, the ESD clamp circuit 310a may comprise only two ESD components (e.g., ESD components 314a and 314n). Thus, the N+ region of

the ESD component 314a is connected to the pad 308, the P+ region of the ESD component 314a is connected to voltage V_{SS}, and the P+ region of the ESD component 314a is connected to the N+ region of the ESD component 314n. In one embodiment of the present invention, the ESD clamp circuit 310a may comprise more than two ESD components (e.g., further comprises a ESD component 314b (not shown) connected between the P+ region of the ESD component 314a and the N+ region of the ESD component 314n). Thus, the N+ region of the ESD component 314b may be connected to the P+ region of the ESD component 314a, and the P+ region of the ESD component 314b may be connected to the N+ region of the diode 314n.

[0053] FIG. 3C is a schematic circuit diagram of an ESD protection circuit according to one embodiment of the present invention. The ESD protection circuit 300c shown in FIG. 3C is similar to the ESD protection circuit 300a shown in FIG. 3A. However, in one embodiment of the present invention, the ESD clamp circuit 310c of the ESD protection circuit 300c comprises, for example but not limited to, one diode 312p connected between voltage V_{DD} and the pad 308, and one ESD component 314p connected between voltage

V_{SS} and the pad 308.

[0054] FIG. 3D is a schematic cross-sectional view illustrating an ESD clamp circuit of an ESD protection circuit according to one embodiment of the present invention. Referring to FIG. 3D, the diode 312p comprises, for example but not limited to, a N+ region and a P+ region formed in a N-well region in a P-type substrate 301. The P+ region of the diode 312p is connected to the pad 308, and the N+ region of the diode 312p is connected to voltage $V_{DD.}$ The ESD components 314p comprises, for example but not limited to, a deep N-well region formed in the P-type substrate 301, a triple P-well formed in the deep N-well region, and an N+ region and a highly doped P-type region formed in the triple P-well region. The N+ region of the ESD component 314p is connected to the pad 308, and the P+ region of the ESD component 314p is connected to voltage V_{SS}.

[0055] It should be noted that, the ESD clamp circuit 310a shown in FIG. 3A and FIG. 3B or the ESD clamp circuit 310c shown in FIG. 3C and FIG. 3D is only illustrate as an exemplary example, and should not be adopted for limiting the scope of the present invention. In the present invention, the ESD clamp circuit may comprise, for example but

not limited to, one or more diode connected between voltage V_{DD} and the pad 308, and one or more ESD component connected between voltage V_{SS} and the pad 308.

[0056] In one embodiment of the present invention, the ESD protection circuit 300a or 300c may be adopted for a RF ESD protection circuit, i.e., the IC 302 comprises a RF IC 302.

[0057] In one embodiment of the present invention, the ESD protection circuit 300a or 300c further comprises an ESD clamp circuit 304. The ESD clamp circuit 304 comprises, for example but not limited to, a PMOS transistor 306a and an NMOS transistor 306b. The gate of the PMOS transistor 306a and an NMOS transistor 306b are connected to the pad 308, the source of the PMOS transistor 306a is connected to the drain of the NMOS transistor 306b, the drain of the PMOS transistor 306a is connected to the voltage V_{DD}, and the source of the NMOS transistor 306b is connected to the voltage V_{SS}.

[0058] Referring to FIG. 3D, the parasitic capacitance the ESD component 314p is associated with the series connection of the parasitic capacitance C4 between the N+ region and the triple P-well region, the parasitic capacitance C5 between the triple P-well region and the deep N-well region, and the parasitic capacitance C6 between the deep

N-well region and the P-type substrate 301. The parasitic capacitance C4 is much less than the parasitic capacitance C5 or C6 since the area of the junction between the N+ region and the triple P-well region is much less than the area of the junction between the triple P-well region and the deep N-well region, or the area of the junction between the deep N-well region and the P-type substrate 301. Therefore, since the parasitic capacitance the ESD component 314p is associated with the series connection of the junction capacitances C4, C5 and C6, the parasitic capacitance the ESD component 314p is less than the junction capacitances C4.

[0059] It should be noted that, when FIG. 3D and FIG. 2B (or FIG. 1B) are under similar process parameters and structure dimensions, the parasitic capacitance C4 is close to the parasitic capacitance C3 (or C1) since the area of the junction between the N+ region and the triple P-well in the ESD component 314p is close to the area of the junction between the N+ region and the P-type substrate 201 (or the area of the junction between the P+ region and the N-well region). Therefore, the parasitic capacitance of the ESD component 314p (less than the junction capacitances C4) is less than the parasitic capacitance C3 of the diode

214 or less than the parasitic capacitance (C1+C2)/m of the series connection of the diodes 114a to 114n. Accordingly, the parasitic capacitance of the ESD clamp circuit 310c is less than that of the diode string 210 or the diode string 110.

[0060] In addition, when FIG. 3B and FIG. 3D are under similar process parameters and structure dimensions, the parasitic capacitance of the series connection of the ESD components 314a to 314n shown in FIG. 3B is less than the parasitic capacitance of the ESD component 314p shown in FIG. 3D. Accordingly, the parasitic capacitance of the ESD clamp circuit 310a is much less than that of the diode string 210 or the diode string 110.

[0061] FIG. 4 is a diagram illustrating the parasitic capacitance of the ESD clamp circuit of the present invention and the conventional diode string versus the number of the ESD components or diodes thereof. In FIG. 4, the uppermost line represents the parasitic capacitance of the conventional diode string 110 including k diodes 112a to 112m (i.e., m=k) and k diodes 114a to 114n (i.e., n=k), wherein k=1, 2, or 3. The middle line represents the parasitic capacitance of the conventional diode string 210 including k diodes 212a to 212m (i.e., m=k) and one diodes 214a,

wherein k=1, 2, or 3. The lowermost line represents the parasitic capacitance of the ESD clamp circuit 310c comprising one diode 312p and one ESD components 314p as shown in FIG. 3D (i.e., k=1), and the ESD clamp circuit 310a comprising k diode 312a to 312m (i.e., m=k) and k ESD components 314a to 314n (i.e., n=k) as shown in FIG. 3D, wherein k=2, or 3. It should be noted that, the ESD clamp circuit 310a or 310c has the lowest parasitic capacitance compared to that of the conventional diode string 110 or 210.

[0062] FIG. 5A is a schematic circuit diagram of an ESD protection circuit according to one embodiment of the present invention. FIG. 5B is a schematic cross-sectional view illustrating an ESD clamp circuit of an ESD protection circuit according to one embodiment of the present invention. The ESD protection circuit 500a shown in FIG. 5A and FIG. 5B is similar to the ESD protection circuit 300a shown in FIG. 3A and FIG. 3B except for that the diodes 312a to 312m of the ESD clamp circuit 310a is replaced by the ESD components 512a to 512m of the ESD clamp circuit 510a.

[0063] FIG. 5C is a schematic circuit diagram of an ESD protection circuit according to one embodiment of the present invention. FIG. 5D is a schematic cross-sectional view illus-

trating an ESD clamp circuit of an ESD protection circuit according to one embodiment of the present invention. The ESD protection circuit 500c shown in FIG. 5C and FIG. 5D is similar to the ESD protection circuit 300c shown in FIG. 3C and FIG. 3D except for that the diodes 312p of the ESD clamp circuit 310c is replaced by the ESD components 512p of the ESD clamp circuit 510c.

[0064] It should be noted that, when FIG. 5D and FIG. 3D are under similar process parameters and structure dimensions, the parasitic capacitance of the series connection of the ESD component 512p shown in FIG. 5D is less than the parasitic capacitance of the ESD component 312p shown in FIG. 3D. Thus, the parasitic capacitance of the ESD clamp circuit 510c is less than that of the ESD clamp circuit 310c. Accordingly, the parasitic capacitance of the ESD clamp circuit 510c is much less than that of the diode string 210 or the diode string 110.

[0065] In addition, when FIG. 5B and FIG. 3B are under similar process parameters and structure dimensions, the parasitic capacitance of the series connection of the ESD components 512a to 512m shown in FIG. 5B is less than the parasitic capacitance of the ESD components 312a to 312m shown in FIG. 3B. Thus, the parasitic capacitance of

the ESD clamp circuit 510a is less than that of the ESD clamp circuit 310a. Accordingly, the parasitic capacitance of the ESD clamp circuit 510a is much less than that of the diode string 210 or the diode string 110.

[0066] Accordingly, since the ESD component is provided for the ESD clamp circuit of the ESD protection circuit of the present invention, the parasitic capacitance of the ESD clamp circuit is much less than that of the conventional diode string. In addition, since the ESD component dose not constructed by the substrate of the ESD clamp circuit of the ESD protection circuit, the problem of the substrate noise may be reduced.

[0067] The foregoing description of the preferred embodiment of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form or to exemplary embodiments disclosed. Accordingly, the foregoing description should be regarded as illustrative rather than restrictive. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments are chosen and described in order to best explain the principles of the invention and its best mode practical application, thereby to enable persons

skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use or implementation contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents in which all terms are meant in their broadest reasonable sense unless otherwise indicated. It should be appreciated that variations may be made in the embodiments described by persons skilled in the art without departing from the scope of the present invention as defined by the following claims. Moreover, no element and component in the present disclosure is intended to be dedicated to the public regardless of whether the element or component is explicitly recited in the following claims.